

Having thus described the preferred embodiment, the invention is now claimed to be:

1. A package mounting integrated circuit chips onto a circuit board comprising:

- 55 an integrated circuit chip having a surface array of input/output pads on one side thereof which array forms a footprint;
- a chip carrier formed of an organic glass filled epoxy dielectric material having first and second opposite surfaces;
- 60 said chip carrier having a coefficient of thermal expansion of at least 17×10^{-6} ppm/c°;
- a first set of bonding pads formed on said first surface of the chip carrier and arranged in an array corresponding with the chip footprint;
- 65 a pattern of conductors on said chip carrier connected to accommodate said input/output pads;

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a first set of solder connections interconnecting the input/output pads on the chip to said first set of bonding pads on the chip carrier;

an encapsulation material encapsulating said first set of solder connections;

a second set of bonding pads formed on the second surface of the chip carrier arranged in an array;

electrically conducting vias extend through the chip carrier connecting said first set of bonding pads to the second set of bonding pads;

a circuit board formed of an organic material having a coefficient of thermal expansion similar to the chip carrier;

a set of electrical connection sites formed on said circuit board and arranged in a pattern corresponding to the pattern of the array of the second bonding pads on said chip carrier;

a second set of solder connections interconnecting the pads of said second set of bonding pads on the chip carrier to the connection sites on the circuit board; and wiring on said circuit board connected to said second set of bonding pads.

2. The package of claim 1 wherein said chip carrier and said circuit board are formed of the same material.

3. The package as defined in claim 1 wherein said first set of solder connections is formed of a higher melting point solder than said second set of solder connections.

4. The package as defined in claim 1 further characterized by first bonding pads being more closely spaced to each other than said second bonding pads.

5. The package as defined in claim 1 wherein the thermal coefficient of expansions of the material of the chip carrier and the material of the circuit board do not differ by more than about 20%.

6. The package as defined in claim 1 wherein the thickness of the conductors on said chip carrier is thinner than the wires of the wiring on the circuit board.

7. A method of mounting integrated circuit chips onto a circuit board comprising the steps of:

providing an integrated circuit chip having a surface array of input/output pads on one side thereof which array forms a footprint;

providing a chip carrier formed of an organic glass filled epoxy dielectric material having first and second opposite surfaces;

said chip carrier having a coefficient of thermal expansion of at least 17×10^{-6} ppm/c°;

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forming a first set of bonding pads on said first surface of the chip carrier arranged in an array corresponding with the chip footprint;

5 providing a pattern of conductors on said chip carrier connected to accommodate said input/output pads;

forming a first set of solder connections between the input/output pads on the chip and said first set of bonding pads on the chip carrier;

10 an encapsulation material encapsulating said first set of solder connections;

forming a second set of bonding pads on the second surface of the chip carrier arranged in an array;

15 forming electrically conducting vias through the chip carrier to connect said first set of bonding pads to the second set of bonding pads;

20 providing a circuit board formed of an organic material having a coefficient of thermal expansion similar to the chip carrier;

forming a set of electrical connection sites on said circuit board arranged in a pattern corresponding to the pattern of the array of the second bonding pads on said chip carrier;

25 forming a second set of solder connections between the pads of said second set of bonding pads on the chip carrier and the connection sites on the circuit board; and

30 forming wiring on said circuit board connected to said second set of bonding pads.

8. The method of claim 7 wherein said chip carrier and said circuit board are formed of the same material.

35 9. The method as defined in claim 7 wherein said first set of solder connections is formed of a higher melting point solder than said second set of solder connections.

10. The method as defined in claim 7 further characterized by first bonding pads being more closely spaced to each other than said second bonding pads.

40 11. The method as defined in claim 7 wherein the thermal coefficient of expansions of the material of the chip carrier and the material of the circuit board do not differ by more than about 20%.

45 12. The package as defined in claim 7 wherein the thickness of the conductors on said chip carrier is thinner than the wires of the wiring on the circuit board.

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13. A package mounting integrated circuit chips onto a circuit board comprising:

an integrated circuit chip having a surface array of input/output pads on one side thereof which array forms a footprint;

a chip carrier formed of an organic dielectric material
and having first and second opposite surfaces;

said chip carrier having a coefficient of thermal expansion of at least about 15×10^{-6} ppm/C°;

a first set of bonding pads formed on said first surface of the chip carrier and arranged in an array corresponding with the chip footprint;

a pattern of conductors on said chip carrier connected to accommodate said input/output pads;

a first set of solder connections interconnecting the input/output pads on the chip to said first set of bonding pads on the chip carrier;

an encapsulation material encapsulating said first set
of solder connections;

a second set of bonding pads formed on the second surface of the chip carrier arranged in an array;

electrically conducting vias extend through the chip carrier connecting said first set of bonding pads to the second set of bonding pads;

a circuit board formed of an organic material having a coefficient of thermal expansion similar to the chip carrier;

a set of electrical connection sites formed on said circuit board and arranged in a pattern corresponding to the pattern of the array of the second bonding pads on said chip carrier;

a second set of solder connections interconnecting the pads of said second set of bonding pads on the chip carrier to the connection sites on the circuit board; and

23 electrically conducting vias extend through the chip
24 carrier connecting said first set of bonding pads to the second
25 set of bonding pads;

26 a set of electrical connection sites formed on said
27 circuit board and arranged in a pattern corresponding to the
28 pattern of the array of the second bonding pads on said chip
29 carrier;

30 a second set of solder connections interconnecting the
31 pads of said second set of bonding pads on the chip carrier to
32 the connection sites on the circuit board; and
33 wiring on said circuit board connected to said second
34 set of bonding pads.

1 17. A package according to claim 16 wherein the thermal
2 coefficient of expansions of the material of the chip carrier and
3 the material of the circuit board do not differ by (more than
4 about 20%.

1 18. A package according to claim 16 wherein said chip
2 carrier and said circuit board are formed of the same material.

1 19. A package according to claim 16 wherein said chip
2 carrier is formed of a glass filled epoxy.

1 20. A package according to claim 16 wherein said chip
2 carrier has a coefficient of thermal expansion of at least about
3 16×10^{-6} ppm/C°.

1 21. A package mounting integrated circuit chips onto a
2 circuit board comprising:

3 an integrated circuit chip having a surface array of
4 input/output pads on one side thereof which array forms a
5 footprint;

6 a chip carrier formed of an organic dielectric material
7 having first and second opposite surfaces;

8 a first set of bonding pads formed on said first
9 surface of the chip carrier and arranged in an array
10 corresponding with the chip footprint;

11 a pattern of conductors on said chip carrier connected
12 to accommodate said input/output pads;

13 a first set of solder connections interconnecting the
14 input/output pads on the chip to said first set of bonding pads
15 on the chip carrier;

16 an encapsulation material encapsulating said first set
17 of solder connections;

18 a second set of bonding pads formed on the second
19 surface of the chip carrier arranged in an array;

20 electrically conducting vias extend through the chip
21 carrier connecting said first set of bonding pads to the second
22 set of bonding pads;

23 a circuit board formed of an organic material having a
24 coefficient of thermal expansion similar to the chip carrier;

25 a set of electrical connection sites formed on said
26 circuit board and arranged in a pattern corresponding to the
27 pattern of the array of the second bonding pads on said chip
28 carrier;

29 a second set of solder connections interconnecting the
30 pads of said second set of bonding pads on the chip carrier to
31 the connection sites on the circuit board; and

32 wiring on said circuit board connected to said second
33 set of bonding pads.

1 22. A package according to claim 21 wherein the thermal
2 coefficient of expansions of the material of the chip carrier and
3 the material of the circuit board do not differ by more than
4 about 20%.

1 23. The package of claim 21 wherein said chip carrier and
2 said circuit board are formed of the same material.

1 24. A package according to claim 21 wherein said chip
2 carrier is formed of a glass filled epoxy.

1 25. A package according to claim 21 wherein said chip
2 carrier is formed of a polyimide.

1 ~~26. A method of mounting integrated circuit chips onto a~~
2 ~~circuit board comprising the steps of:~~

3 ~~providing an integrated circuit chip having a surface~~
4 ~~array of input/output pads on one side thereof which array forms~~
5 ~~a footprint;~~

6 ~~providing a chip carrier formed of an organic~~
7 ~~dielectric material having a coefficient of thermal expansion of~~
8 ~~at least about 15×10^{-6} ppm/c., and having first and second~~
9 ~~opposite surfaces;~~

10 ~~forming a first set of bonding pads on said first~~
11 ~~surface of the chip carrier arranged in an array corresponding~~
12 ~~with the chip footprint;~~

13 ~~providing a pattern of conductors on said chip carrier~~
14 ~~connected to accommodate said input/output pads;~~

15 ~~forming a first set of solder connections between the~~
16 ~~input/output pads on the chip and said first set of bonding pads~~
17 ~~on the chip carrier;~~

18 ~~encapsulating said first set of solder connections;~~

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8 providing a chip carrier formed of an organic
9 dielectric material having a coefficient of thermal expansion
10 similar to the circuit board, said chip carrier having first and
11 second opposite surfaces;

12 forming a first set of bonding pads on said first
13 surface of the chip carrier arranged in an array corresponding
14 with the chip footprint;

15 providing a pattern of conductors on said chip carrier
16 connected to accommodate said input/output pads;

17 forming a first set of solder connections between the
18 input/output pads on the chip and said first set of bonding pads
19 on the chip carrier;

20 encapsulating said first set of solder connections with
21 an encapsulation material;

22 forming a second set of bonding pads on the second
23 surface of the chip carrier arranged in an array;

24 forming electrically conducting vias through the chip
25 carrier to connect said first set of bonding pads to the second
26 set of bonding pads;

27 forming a set of electrical connection sites on said
28 circuit board arranged in a pattern corresponding to the pattern
29 of the array of the second bonding pads on said chip carrier;

30 forming a second set of solder connections between the
31 pads of said second set of bonding pads on the chip carrier and
32 the connection sites on the circuit board; and

33 forming wiring on said circuit board connected to said
34 second set of bonding pads.

1 30. A method according to claim 29 wherein said chip
2 carrier has a coefficient of thermal expansion of at least about
3 16×10^{-6} ppm/C°.

1 ~~31. A method according to claim 29 wherein said chip~~
 2 ~~carrier has a coefficient of thermal expansion of at least about~~
 3 ~~17×10^{-6} ppm/C°.~~

1 32. A method according to claim 29 wherein said chip
 2 carrier is formed of a glass filled epoxy.

1 33. A method according to claim 29 wherein said chip
 2 carrier is formed of a polyimide.

1 34. A method of mounting integrated circuit chips onto a
 2 circuit board comprising:

3 providing an integrated circuit chip having a surface
 4 array of input/output pads on one side thereof which array forms
 5 a footprint;

6 providing a chip carrier formed of an organic
 7 dielectric material having first and second opposite surfaces;

8 forming a first set of bonding pads formed on said
 9 first surface of the chip carrier and arranged in an array
 10 corresponding with the chip footprint;

11 providing a pattern of conductors on said chip carrier
 12 connected to accommodate said input/output pads;

13 forming a first set of solder connections
 14 interconnecting the input/output pads on the chip to said first
 15 set of bonding pads on the chip carrier;

16 encapsulating said first set of solder connections;

17 forming a second set of bonding pads formed on the
 18 second surface of the chip carrier arranged in an array;

19 forming electrically conducting vias extend through the
 20 chip carrier connecting said first set of bonding pads to the
 21 second set of bonding pads;

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22 providing a circuit board formed of an organic material
23 having a coefficient of thermal expansion similar to the chip
24 carrier;

25 forming a set of electrical connection sites on said
26 circuit board and arranged in a pattern corresponding to the
27 pattern of the array of the second bonding pads on said chip
28 carrier;

29 forming a second set of solder connections
30 interconnecting the pads of said second set of bonding pads on
31 the chip carrier to the connection sites on the circuit board;
32 and

33 forming wiring on said circuit board connected to said
34 second set of bonding pads.